


[Home](#) | [Login](#) | [Logout](#) | [Access Information](#) | [Alt](#)

Welcome United States Patent and Trademark Office

Search Results

[BROWSE](#)[SEARCH](#)[IEEE XPLORE GUIDE](#)

Results for "((((width, length, size) <near/7> (tag*, bit*) <and> (parallel*, concurrent*, pipe..."

☒ e-mailYour search matched **11** of **302** documents.A maximum of **100** results are displayed, **25** to a page, sorted by **Relevance** in **Descending** order.

» Search Options

[View Session History](#)[New Search](#)

» Key

IEEE JNL IEEE Journal or Magazine

IEEE JNL IEE Journal or Magazine

IEEE CNF IEEE Conference Proceeding

IEEE CNF IEE Conference Proceeding

IEEE STD IEEE Standard

Modify Search

((((width, length, size) <near/7> (tag*, bit*) <and> (parallel*, concurrent*, pipelin*))

[Search](#)☐ Check to search only within this results set

Display Format:



Citation



Citation & Abstract

[view selected items](#)[Select All](#) [Deselect All](#)

- ☐ **1. Microarchitectural wire management for performance and power in partitioned architectures**
Balasubramonian, R.; Muralimanoahar, N.; Ramani, K.; Venkatachalapathy, V.;
[High-Performance Computer Architecture. 2005. HPCA-11. 11th International Symposium on](#)
12-16 Feb. 2005 Page(s):28 - 39
Digital Object Identifier 10.1109/HPCA.2005.21
[AbstractPlus](#) | Full Text: [PDF](#)(208 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **2. A C to HDL compiler for pipeline processing on FPGAs**
Maruyama, T.; Hoshino, T.;
[Field-Programmable Custom Computing Machines. 2000. IEEE Symposium on](#)
17-19 April 2000 Page(s):101 - 110
Digital Object Identifier 10.1109/FPGA.2000.903397
[AbstractPlus](#) | Full Text: [PDF](#)(696 KB) IEEE CNF
[Rights and Permissions](#)
- ☐ **3. High-throughput LDPC decoders**
Mansour, M.M.; Shanbhag, N.R.;
[Very Large Scale Integration \(VLSI\) Systems. IEEE Transactions on](#)
Volume 11, Issue 6, Dec. 2003 Page(s):976 - 996
Digital Object Identifier 10.1109/TVLSI.2003.817545
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(2481 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ **4. Successive superposition: a technique for the exact modeling of deterministic packet queue**
Picker, D.; Fellman, R.D.;
[Parallel and Distributed Systems. IEEE Transactions on](#)
Volume 7, Issue 10, Oct. 1996 Page(s):1106 - 1120
Digital Object Identifier 10.1109/71.539741
[AbstractPlus](#) | [References](#) | Full Text: [PDF](#)(1376 KB) IEEE JNL
[Rights and Permissions](#)
- ☐ **5. Integration of hierarchical test generation with behavioral synthesis of controller and data p**
Bhatia, S.; Jha, N.K.;
[Very Large Scale Integration \(VLSI\) Systems. IEEE Transactions on](#)
Volume 6, Issue 4, Dec. 1998 Page(s):608 - 619
Digital Object Identifier 10.1109/92.736134

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(240 KB\)](#) IEEE JNL
[Rights and Permissions](#)

- ☐ 6. **Behavioral synthesis of fault secure controller/datapaths based on aliasing probability analysis**
 Lakshminarayana, G.; Raghunathan, A.; Jha, N.K.;
[Computers, IEEE Transactions on](#)
 Volume 49, Issue 9, Sept. 2000 Page(s):865 - 885
 Digital Object Identifier 10.1109/12.869319

[AbstractPlus](#) | [References](#) | Full Text: [PDF\(532 KB\)](#) IEEE JNL
[Rights and Permissions](#)

- ☐ 7. **A small, fast and low-power register file by bit-partitioning**
 Kondo, M.; Nakamura, H.;
[High-Performance Computer Architecture, 2005. HPCA-11. 11th International Symposium on](#)
 12-16 Feb. 2005 Page(s):40 - 49
 Digital Object Identifier 10.1109/HPCA.2005.3

[AbstractPlus](#) | Full Text: [PDF\(408 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ 8. **High-performance decoders for regular and irregular repeat-accumulate codes**
 Mansour, M.M.;
[Global Telecommunications Conference, 2004. GLOBECOM '04. IEEE](#)
 Volume 4, 29 Nov.-3 Dec. 2004 Page(s):2583 - 2588 Vol.4
 Digital Object Identifier 10.1109/GLOCOM.2004.1378472

[AbstractPlus](#) | Full Text: [PDF\(1025 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ 9. **Efficient processing of color image sequences using a color-aware instruction set on mobile processors**
 Jongmyon Kim; Wills, D.S.;
[Application-Specific Systems, Architectures and Processors, 2004. Proceedings. 15th IEEE International Symposium on](#)
 2004 Page(s):137 - 149
 Digital Object Identifier 10.1109/ASAP.2004.1342465

[AbstractPlus](#) | Full Text: [PDF\(509 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ 10. **A novel round function architecture for AES encryption/decryption utilizing look-up table**
 Jhing-Fa Wang; Sun-Wei Chang; Po-Chuan Lin;
[Security Technology, 2003. Proceedings. IEEE 37th Annual 2003 International Carnahan Conference on](#)
 14-16 Oct. 2003 Page(s):132 - 136
 Digital Object Identifier 10.1109/CCST.2003.1297549

[AbstractPlus](#) | Full Text: [PDF\(1456 KB\)](#) IEEE CNF
[Rights and Permissions](#)

- ☐ 11. **Test scheduling and controller synthesis in the CADDY-system**
 Rudolph, M.; Neher, M.; Rosenstiel, W.;
[Design Automation, EDAC, Proceedings of the European Conference on](#)
 25-28 Feb. 1991 Page(s):278 - 282
 Digital Object Identifier 10.1109/EDAC.1991.206408

[AbstractPlus](#) | Full Text: [PDF\(408 KB\)](#) IEEE CNF
[Rights and Permissions](#)

[Help](#) [Contact Us](#) [Privacy](#)

© Copyright 2006 IEEE

